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Miniaturization and Packaging Concept in Power Amplifier using GaN device for Space Applications

Kamaljeet Singh*, Dinesh Kumar, AV Nirmal, SV Sharma

ABSTRACT

This article details the concept of using gallium nitride devices for high power application in the transmitter chain. The issue of thermal management is detailed along with the possible configuration yielding the size reduction with the proposed approach. Practical approach of the same is demonstrated for development of power amplifier chain for deep space mission requirements along with the comparative analysis with the prevalent topologies. SSPA designed using GaN device can replace expensive TWTA and have the added flexibility of designing at desired frequencies with a single device.

Keywords : Power amplifier, Gallium Nitride (GaN), matching, High-electron-mobility-transistor, packaging, thermal resistance

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INTRODUCTION

High power amplifiers are widely used in terrestrial base systems and satellite communication systems. Solid state devices for power amplifier (SSPA) are being employed for high power outputs [1]. In comparison to TWTs the major advantages associated with SSPA are overcoming warm up time, cathode wear out, out gassing, vacuum tube contamination, and thermionic emission failures. Main consideration for microwave data transmitter is to have negligible distortion and high linearity so as to prevent the regeneration of side lobes [2]. Further for space based applications, cost and weight are important factors which necessitate the implementation of amplifier chain using solid state devices. In case of satellite system, power amplifier is an critical component as reliable link margin and satellite operations are directly linked with its performance [3-4]. Major limitation in the solid state technology is the limited efficiency and power. The recent advances in this field and availability of space grade devices successfully overcome this limitation. Mostly Gallium Arsenide (GaAs) HEMT technology is employed due to lower DC power consumption but it can provide limited output power for a given die size. High saturated power requires the usage of large periphery devices resulting in low impedances which in turn causes mismatch losses, low efficiency, low output power and higher parasitics.

In comparison of GaAs MESFET technology, high operating voltages and high power densities are possible with the wide-bandgap RF devices. Latest generation of Silicon Carbide (SiC) and gallium nitride (GaN) devices offer improvement in efficiency, heat load tolerance, low leakage currents,

high breakdown voltages and higher cut-off frequency . These devices offer to build wide bandwidths and capable of achieving improved flatness over the band. Even though SiC devices are having superior performance but not matured enough to be implemented in space application. LDMOS technology is also gaining popularity but compared to LDMOS, GaN offers lower operating costs, simpler cooling, smaller footprint, broader choice, higher efficiency and easier matching. GaN technology is having inherent high power density which generates high power in both CW and pulsed mode of operation at frequency beyond microwave range due to high electron mobility, high breakdown voltage and high temperature operations associated with it. GaN has emerged as the choice for high-power switches and amplifiers and the main applications of these devices are in the field of ISM, wireless, commercial and space [5]. The main challenge in this technology is the issue of thermal management in actual conditions due to smaller thermal footprint. Recent advances in these devices overcome associated problems such as material defects, current collapsed and thermal management issue. Package selection plays an important role as it provides the basic interface of the device to the remaining components of the system along with effective connections with the heat sink. The requirements of power amplifier for deep space missions are compact size, good efficiency, distortion free, high linearity. Existing topologies implemented in the power amplifier is having low efficiency resulting in thermal issues, increased size and cost due to auxiliary circuits. This article details the thermal issue associated with the power amplifier, theoretical concept, assembly and package considerations, biasing and implementation methodology of power amplifiers for future deep space mission requirements.

MATERIALS AND METHOD

Packaging Considerations

Package is an essential component for achieving high performance at high frequencies. Package produces considerable influence on the overall performance of the power amplifier. Compared to package it is preferable to use die format as it is much cheaper and more flexible. Further it possible to put internal matching network and load more than one transistor in the package. But this arrangement needs to predict accurately the package parasitic and poses difficulty in matching due to lack of large signal parameters. Internally matched packaged device is generally chosen for the ease of matching and circumventing need for finding out associated parasitic.

Demands for higher reliability, better performance and lower system costs are driving the development of complex, high density packaging technologies. Several factors are responsible for the package selection such as intended application, size, reliability, repeatability and most importantly thermal dissipation and thermal coefficient of expansion of the device. Packages commonly employed are QFN, TO-272 and ceramic keeping into consideration of

electrical performance, environmental protection and shielding. The other criteria for the selection of material is the maximum operating temperature (MOT) which is related with the insertion loss and circuit design to take care of this aspect.

Device or chip is attached to the package with adhesives or solders. Epoxies and low melting temperature solders are preferable keeping into consideration the thermal aspects. Die is attached to the Kovar material using silver based epoxy resulting in better heat transfer due to higher thermal conductivity of silver. Compared to plastic packages having low thermal conductivity, high power transistor uses BeO based ceramic having better thermal conductivity. Ceramic materials are having stable dielectric properties over wide frequency range, good mechanical strength, good moisture resistance, capability of handling high processing temperature and provide good hermiticity. Package is further attached to the PCB and copper filled thermal vias under the centre

pad of package is an effective technique for dissipation of heat. PCB selection at higher frequency and power amplifier applications plays an important role in the power amplifier performance. The major parameters for the selection of PCB materials are dielectric constant, dissipation factor, and thermal conductivity, temperature coefficient of dielectric constant, copper surface roughness, and material thickness. Keeping above consideration, PCB material having ceramic filled PTFE with woven glass reinforcement is employed which is having low CTE, better electrical performance and higher thermal conductivity. Further, PCB with openings for heat sink with machined pedestals and coined PCBs can also solve higher power dissipation. These techniques provide lower thermal resistance from the package through the PCB to the external heat sink. Attachment of PCB to heat sink can be carried out using mechanical screw-down fasteners, sweat soldering, or applying thermally and electrically conductive adhesives (TECA). The PCB is attached using TECA on the aluminium plate for RF ground as well as acting as a heat sinker [6].

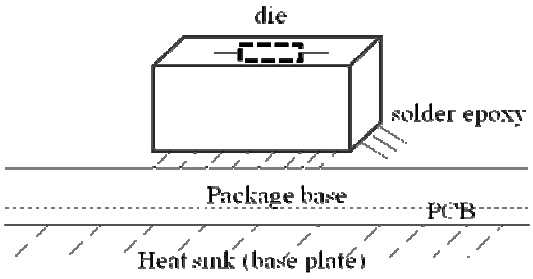

Fig 1: Complete assembly sketch of power amplifier die

Overall package loss is more as parasitic introduced by the packages are considerably higher compared to the die losses. The reduction in the losses can be achieved by arranging/routing the die, reduction in common source inductance, low inductance gate and low internal parasitic inductances. The selection of the package depends on the pin configuration and layout of the same to fully utilize the technology benefits.

Thermal Management Concept

The utmost parameter in the power amplifier circuit deals with the thermal management so as to remove the generated heat efficiently. Heat removal is associated with the maintenance of channel temperature and can be carried out by conduction, convection, radiation or combination of all three. The rise in channel temperature can be represented as

$$T_j = R_{th} P_{diss} + T_c \quad \text{.....(1)}$$

where R_{th} is junction thermal resistance, P_{diss} is average dissipated power, T_c is case temperature

As in the case of standard power devices, the heat is dissipated near the surface, under the gate and near the drain end (Fig 1) so equation (1) is modified as

$$T_j = P_{diss}(R_{th,chip} + R_{th,solder} + R_{th,mount} + R_{th,PCB}) + T_c \quad \text{...(2)}$$

Higher thermal conductivity results in lower thermal resistance resulting in effective heat removal due to faster heat dissipation. Considering device thickness to be small compared to dimension of the device, the heat flow in the vertical column can be represented as R_{COL} instead of R_{th} for the device thickness of 'T' and given as

$$R_{COL} = \frac{T}{K_{TH} \times Area} \quad \text{……..(3)}$$

where R_{COL} is vertical column thermal resistance, K_{TH} is thermal conductivity of the material

So $$R_T = R_{COL} + R_{th,solder} + R_{th,mount} + R_{th,PCB} \quad \text{…..(4)}$$

Alternatively, in terms of time‘t’ the equation 1 can be written as

$$T_j = P_{diss} R_T \left[\frac{4}{\pi^{3/2}}\right]\left[\frac{t}{\tau_T}\right]^{1/2} + T_A \quad \text{……(5)}$$

where τ_T is the total thermal constant $=\tau_{die}+\tau_{solder}+\tau_{mount}+\tau_{PCB}$ where $\tau_{die}= \left(\frac{2T}{\pi}\right)^2\left[\frac{\rho.C}{K_{TH}}\right]$

where ρ is the density ,C is the specific heat and T_A is the ambient temperature.

Table-1: Parameters comparison of power devices

Parameters	Si Device	GaAs Device	GaN Device
K_{TH}(W/gmºC)	1	0.44	1.3
ρ (gm/cc)	2.33	5.31	6.15
Specific Heat (J/gmºC)	0.7	0.35	0.49
Bandgap	1.1	0.35	3.4
Dielectric Constant	11.4	12.8	9.5
Mobility (μ)	1300	5000	1500

The major advantages associated with the GaN devices are easy to match, reliable, rugged, better bandwidth, reduced cooling requirement. The performance analysis of GaN devices are listed in the below Table-2.

Table-2: Analysis of the GaN performance

Parameters	Enabling Feature
High Linearity	HEMT Topology
High critical field	High breakdown voltage
High Frequency	High electron mobility
High Efficiency	High operating voltage
High power density	Wide bandgap
High thermal conductivity	Conducting heat efficiently

The above table shows that the GaN is better choice for power amplifier compared to GaAs as they are capable of operating with ten times the power density of GaAs devices and are having melting temperature around 2500º C.

In case of deep space mission, power amplifiers are designed to keep the junction temperature of all active devices within 110°C. About 5°C temperature rise is assumed due to thermal resistance in the heat flow path from heat sink to device case. Cigraflex material is generally used for attachment so as to dissipate heat more effectively.

Power Amplifier Miniaturization using GaN device

Standard power amplifier employs FET based devices at higher frequencies to achieve the desired output power. The approach of single stage to achieve desired output power yields thermal as well as reliability issues.

Table-3: Major specifications for various transmitters

Specifications	S-band (2 GHz)	Deep space missions (2GHz) Moon Mars		Proposed (2 GHz)
Device Driver stage Final stage	AT42070 (BJT) FLLI77E (FET)	AT42070 (BJT) FLL177E (FET)+ TGF4118 (HFET)	AT42070 (BJT) FLL177E (FET) + TGF4118 (HFET)+TWTA	EMM5080VFS+TGA2578+CGHV22200 GaN(IM)
Package	Metal-ceramic hermetic	Die	Die	Surface mount ceramic
Power requirement	8V,320 mA	8V,1.0A	28V,400mA	50V,1.0A
Operating power	30.55dBm@20dBm	37 dBm@30.5 dBm	37 dBm@27 dBm	53dBm@40 dBm
Gain (dB)	10.5	6.5	17	13
Efficiency (%)	17.5	30	25	>40
Operating Temperature° C	-10 to +50	-25to +55	-15 to +55	-25 to +55
Substrate (ε_r)	RT-Duroid (10.2)	RT-Duroid (10.2)	RT-Duroid (10.2)	RT-Duroid (10.2)
Size (mm^2)	45×30	45×30	45×30	45×30

Alternatively chain concept, corporate or radial approach is implemented to achieve desired output power by combining two or more transistors yielding better input and output impedance match with ripple free gain characteristics. Power amplifier can be operated in low, medium and high power region whereas linear and medium ranges is having linear operation (class-A) and high power region is operated at 1-dB compression point (class-B). The efficiency is dictated by the class of operation and specific to the application (linearity, inter-modulation, interferences). Class-D,E,F,J are supposed to achieve higher efficiency but they are operated in switched mode and needs resonators at the output. So Class-AB operation is carried out to obtain high efficiency and better linearity. Bias circuit also plays an important role as excessive gate current shorten the device life and to avoid such phenomena appropriate gate resistance must be used keeping into consideration of linearity and power performance. RC networks at the bias are to be employed to prevent video oscillations. A combination of diode compensation in the bias network and thermopads are used to control the gain variation over the temperature. Driver stage preceding the power amplifier is designed to provide output drive having substantial gain. This is done by having conjugate matching at the input and output of the device based on the small signal design approach. Dies are cascaded in the driver amplifier stages to achieve the desired performances. In power amplifier, the device is drive into compression (1-dB compression) so as to achieve power gain and output power at the desired frequency to achieve higher PAE. Comparison of the transmitter for various bands is shown in Table-3 along with the proposed configuration. In the case of existing topologies, limitation of output power is overcome by combining several devices. [7, 8]

Large signal S-parameters are used to obtain the desired output power and in case of unavailability of the same load and source pull measurement techniques are employed to achieve the same. Further the choice of substrate also plays an important role so as to carry the power from the device. The maximum average power which can be handled is given as

$$P_m = \frac{\theta}{\Delta T} \qquad \text{.....(6)}$$

where ΔT is the temperature rise above ambient and is inversely proportional to K_{TH}.

Selection crtieria and construction

Selection of the device is most important criteria to achieve the optimum and desired performance. GaN HEMT device is having large material band gap which permits them to be operated at high drain voltages and high power density within small size. Basically GaN device on Si and SiC are employed keeping into considerations various parameters as tabulated in Table-4.

Table-4: Major specifications for various bands

Parameters	Si	SiC
Heat Conduction	Good	Very good
Large aperture conversion	Fair	Very good
Crystal quality	Very good	Fair
Growth layer quality	Very good	Fair
Current density	Low	High
Cost	Low	High

Heat dissipation in SiC is faster compared to Si as thermal expansion coefficient of SiC is 4.6×10^{-6}/K matches with GaN which is having an average expansion coefficient of 4.9×10^{-6}/K from 25º C to 1000º C. This results in better cooling of device due to efficient heat removal [9].

The key consideration for the development of GaN HEMT is the selection of the base material. A crystal wafer such as sapphire, SiC or Si is employed as a base substrate and GaN along with AlGaN are formed sequentially using MBE or MOCVD as shown in Fig 2.

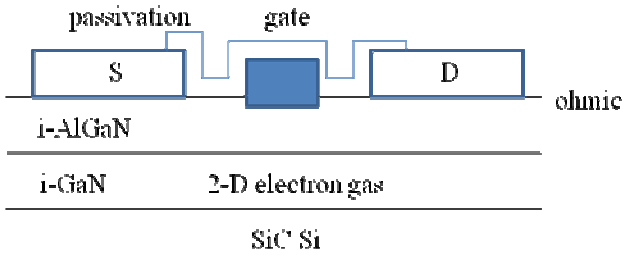

Fig 2: Generic structure of GaN device

The dislocation density of the HEMT structure as shown above on Si and SiC are $8\times10^{8}cm^{-2}$ and $2\times10^{8}cm^{-2}$ respectively and after prolonged annealing the samples on SiC are unaffected which indicates their superiority in high temperature and high-power applications.

Development approach

The targeted application of the proposed methodology is to demonstrate compact and efficient system so as to reduce the

overall size of the on-board SSPA for deep space mission. Table-5 concisely bought out the comparison of the targeted approach.

The input and output impedance matching circuit for MARS mission is realized on the RT Duroid^{R} board with relative dielectric constant of 10.2 and substrate thickness of 1.27 mm (50 mils). The main steps for the realization of the power amplifiers are:

Selection of the device

- Selection of bias and biasing arrangement
- Optimum source and load impedances
- Power contours at desired frequencies
- Transformation for raising load resistance to 50 Ω
- Input and output matching network

Table-5 Overview of the various on-board S-band power amplifier and proposed system

Parameters	LEO mission	Moon mission	Mars mission	Proposed (Deep Space)
Orbit (kms)	800	~ 406700	220-400 $\times10^{6}$	>400$\times$ 10^{6}

Frequency (GHz)	2.2	2.23	2.22	2.22
Operating power @ 1-dB compression at 25°C	1W(33 dBm)	5W(37 dBm)	210 W(53.22 dBm)	200W(53 dBm)
Device	GaAs FET (FLL177ME)	GaAs HFET	GaAs FET/TWTA	GaN on SiC
Remarks	Require tuning	Multiple stages Reduce efficiency	Multiple stages Reduce efficiency	Compact High efficiency

The proposed deep space mission require driver stage to increase the power from -10 dBm to 16 dBm followed by GaN power amplifier to increase it further to +40 dBm.[10, 11] Proposed GaN HEMT devices are operated at higher voltages which increase device optimum impedances and lowers the device parasitic capacitances for a given output power capability. RT Duroid (3010) with ε_r=10.2 is chosen for the present realization so as to realize compact structure with better RF performance.

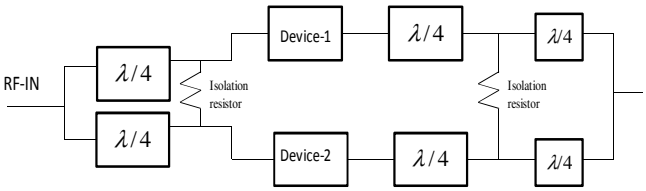

Fig3: Proposed Architecture

Power divider and combiner with isolation resistor as well as mismatch at lower end of frequency to be carried out to curtail oscillations and achieve optimum performance as shown in Fig 3 with the selected internally matched device (IM GaN). Single device is characterized with different input levels and loads to find out the optimum conditions without using the load-pull technique followed by the arrangement as shown above. The overall concept drastically reduces the need for multiple stages while meeting the desired specifications.

CONCLUSION

This article details the theoretical , comparative aspects of the power amplifier and proposes the concept of implementing the state of the art GaN devices for power amplifier chain of SSPA of deep space mission so as to achieve efficiency of >40% and size reduction of around 50% from the existing topology. The article demonstrates achieving higher power density with a single chip whereas equivalent-power GaAs amplifier comprises of multiple chips to achieve the same functionality. Basic concepts of power amplifier and comparison of various high power devices are detailed in this article. Further comparison of the existing topologies with the proposed topology is

carried out.

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Kamaljeet Singh has obtained M. Tech (Microwaves) from Delhi University in 1999 and awarded PhD in 2010. He joined ISRO Satellite center, Bangalore in 1999 where he worked in GEO-receiver. From August 2006 – Feb 2016 he was posted in Semi- Conductor Laboratory, Chandigarh and worked in the areas of RF-MEMS and sensors. He is presently working in SEG group at ISAC.

Dinesh Kumar has obtained B. Tech (E&C) from B.I.T Sindri in 1988. He joined ISRO Satellite Center, Bangalore in 1993. He has been working in Communication Microwave Group. He is working for TTC Transponder for spacecraft. His expertise is in Telemetry Transmitter design in S & X bands for LEO and deep space mission like MARS and Chandrayaan. He has designed & delivered

more than 50 transmitters for LEO and 4 for deep space mission. All has performed flawlessly. He is presently working as Dy. Project Director for RISAT-2A satellite.

A V Nirmal obtained his B.E in Mechanical Engineering. From Kerala University in 1984. He joined VSSC, Trivandrum in 1984 and has been working in ISAC since 2004. He is credited with productionzation and delivering of all sub-systems of IRS and Geosat missions. He was involved in the design and development of various mechanical systems for both Launch vehicle and satellites and establishment of test facilities. He is presently working as Group Director, Systems Engineering Group, ISRO Satellite Centre

Dr S V Sharma is Aluminous of IISc and working in ISRO for the more than 30 Years and contributed significantly in design, development and fabrication of Satellite in various capacities in his service. Presently working as Deputy Director, ISRO Satellite Centre, Bangalore, In-charge of realization of all the flight hard wares. He spear headed ISROs ambitious program of indigenization of components and materials used for space application.