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# Design and Implementation of a Bridgeless Interleaved Boost Converter for Plug- in Hybrid Electric Vehicles

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**ABSTRACT**
*Hybrid Electric Vehicles (HEVs) employs an AC-DC power electronic converter at the front charging end of the vehicle. This converter induces harmonics and distorts the supply current due to the presence of non-linear devices in its topology. Moreover, it leads to poor supply factor and degrades the efficiency of the system. Therefore, it is vital to develop a Power Factor Correction (PFC) circuit to enhance the effective performance of the charger. This paper mainly focuses on the simulation and prototype implementation of a two-phase Bridgeless Interleaved Boost Converter for improving the supply power factor. Simulation o fthe proposed circuit is acrried out uisng MATLAB/SIMULINK. Experimental studies are carried out to verify the simulation results.*

**Keywords :** Hybrid Electric Vehicles, AC-DC Converter, Bridgeless Interleaved, Power Factor Correction

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## INTRODUCTION

The supply current drawn by the HEV chargers at the charging end has higher harmonic content due to the presence of non-linear devices like diodes and MOSFETs in the power conditioning circuitry [1][2][3].This supply current has to be shaped by curtailing the harmonics, considerably, to low levels inorder to achieve unity power factor [4].

The classical boost topology utilizes diode bridge rectifier to rectify the AC input to DC, followed by the DC-DC boost converter [5][6][7]. At high power levels, this topology suffers due to the increased DBR losses which significantly degrades the efficiency [8]. This stems to a problem to be dealt with when huge amounts of heat is dissipated in a limited area. Due to these limitations, this topology is suited for a low to medium power range of 1kW [9][10]. For power rating greater than 1kW, parallel connection of power devices are carried out to generate higher output power in order to reduce the stress across the devices [11] [12].

A Bridgeless topology, eliminating the losses due to a rectifier input bridge, is indeed an optimal solution for applications >1kW [13]. Thus, the Bridgeless Interleaved boost AC-DC converter with PFC, featuring increased output power efficiency and reduced harmonics, proves efficient for implementation at the charging end in Hybrid Electric Vehicles.

## MATERIAL METHOD

### BRIDGELESS INTERLEAVED BOOST CONVERTER

### Circuit Operation

To analyse the circuit operation, the input line cycle is studied under 2 half cycles, the positive half cycle and the negative half cycle [14]. The circuit diagram of the BLIL topology is as follows:

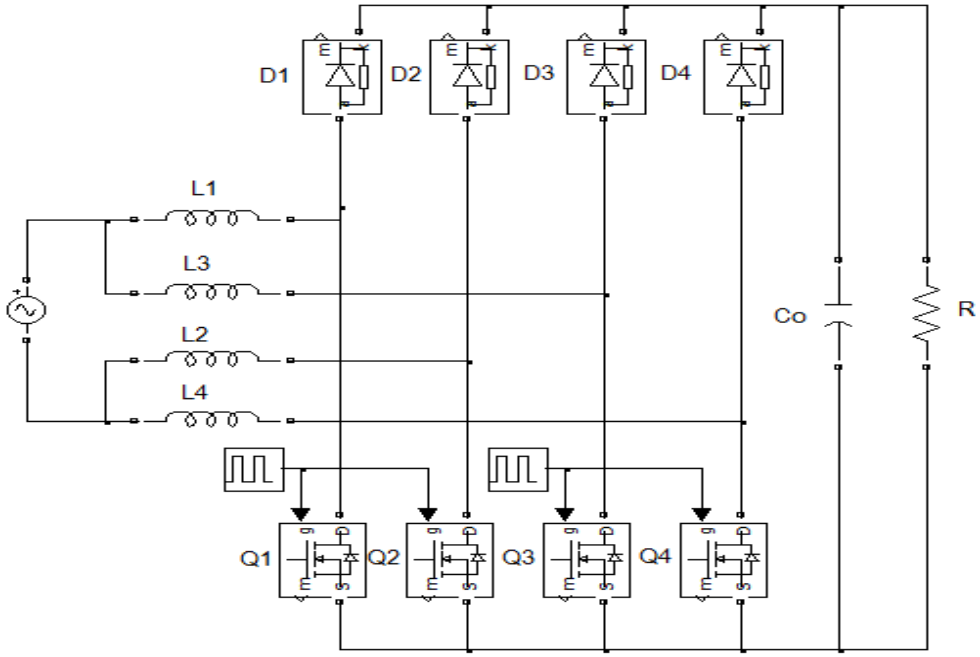


**Figure 1**. Bridgeless Interleaved Boost Topology

### Positive Half Cycle Operation

During the positive half cycle of the supply, the switches $Q_1$ and $Q_2$ are triggered ON. Current traces the path $L_1$ - $Q_1$ - $Q_2$ - $L_2$, and returns to the line storing energy in $L_1$ and $L_2$. When $Q_1$ and $Q_2$ are switched OFF, energy stored in $L_1$ and $L_2$ is released. Current flows through the freewheeling diode $D_1$, through the load and returns to the AC supply through the internal body diode of $Q_2$.

During the interleaving operation, switches $Q_3$ and $Q_4$ are triggered with a phase delay of 180 degrees [14]. The switches $Q_3$ and $Q_4$ are triggered ON thereby storing energy in $L_3$ and $L_4$ through the path $L_3$ -$Q_3$ - $Q_4$ - $L_4$. When $Q_3$ and $Q_4$ are switched OFF, freewheeling action is acheived through $D_3$ – load and .

### Negative Half Cycle Operation

During the negative half cycle of the supply, the switches $Q_1$ and $Q_2$ are triggered ON. Current traces the path $L_2$ - $Q_2$ - $Q_1$ - $L_1$, and returns to the line storing energy in $L_2$ and $L_1$. When $Q_1$ and $Q_2$

are switched OFF, energy stored in $L_2$ and $L_1$ is released. Energy is fedback to the source by the freewheling diode $D_2$.

During the interleaving operation, switches $Q_3$ and $Q_4$ are triggered with a phase delay of 180 degrees. The operation of this mode is – switches $Q_3$ and $Q_4$ are triggered ON thereby storing energy in $L_3$ and $L_4$ through the path $L_4$ -$Q_4$ - $Q_3$ - $L_3$ [14]. When $Q_3$ and $Q_4$ are switched OFF, the energy stored in $L_4$ and $L_3$ is released. Charge is discharged through the diode $D_4$ - load and returns to the mains through the body diode of $Q_3$ [15].

## DESIGN ASPECTS OF THE PROPOSED CONVERTER

The controlling parameter duty ratio (D) of a boost converter is given by [16]

$$D = \frac{V_{out} - V_{in}}{V_{out}} \quad \textbf{(1)}$$

where,
- Output Voltage $V_{out}$
- Input Voltage (Supply Voltage) $V_{in}$

The inductance of the boost - inductor is determined using the expression as in [16]

$$L = \frac{V_{in} \text{ x } D}{I_{ripple} \text{ x } f} \quad \textbf{(2)}$$

where,
- Inductance L
- Switching frequency f
- Inductor current ripple. $I_{ripple}$

The value of capacitance (C) for the filter at the load end is given as the following equation in [16]

$$C = \frac{V_{out} \text{ x } D}{f \text{ x } \Delta V \text{ x } R} \quad (3)$$

where,
- Output voltage ripple $\Delta V$
- Resistance R

## RESULTS AND DISCUSSION

### SIMULATION RESULTS

### Parameters

**Table 1:** Simulation Parameters of the Classical Boost Rectifier Circuit

| | |
|---|---|
| Input voltage | 20 V |
| Supply frequency | 50 Hz |
| L | 131.575 µH |
| R | 52.63 Ω |

| | |
|---|---|
| C | 850 µF |
| Switching frequency | 25 kHz |

**Table 2:** Simulation Parameters of the proposed Bridgeless Boost Rectifier Circuit

| | |
|---|---|
| Input voltage | 20 V |
| Supply frequency | 50 Hz |
| L | 131.575 µH |
| R | 52.63 Ω |
| C | 850 µF |
| Switching frequency | 25 kHz |

**Graphical Results**

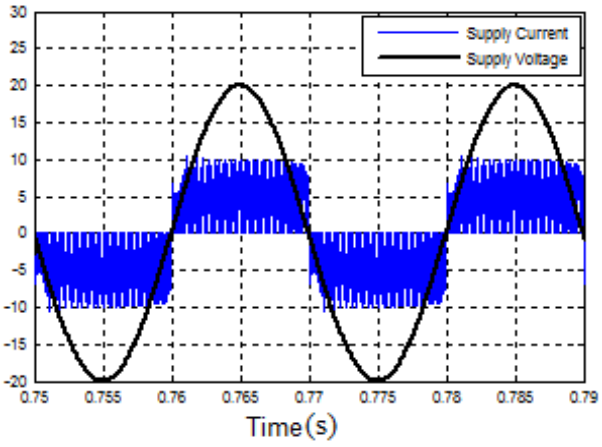


**Figure 2**. Input Current and Voltage waveforms for the classical Boost Rectifier circuit

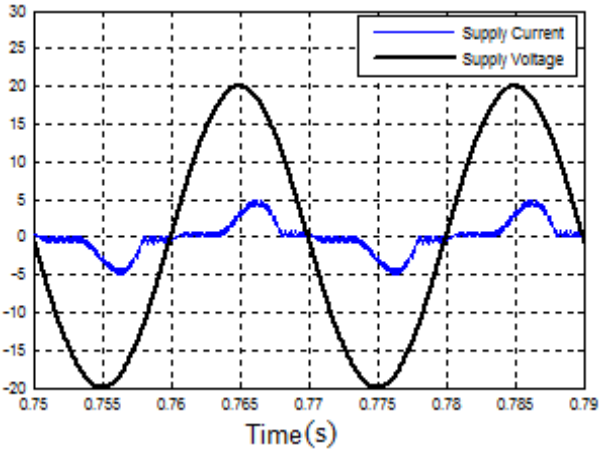


**Figure 3.** Input Current and Voltage Waveforms for the proposed Bridgeless Boost Rectifier Circuit

Figures 2 & 3 show that the Classical boost rectifier has higher amount of harmonics in the supply current waveform than the proposed Bridgeless converter.

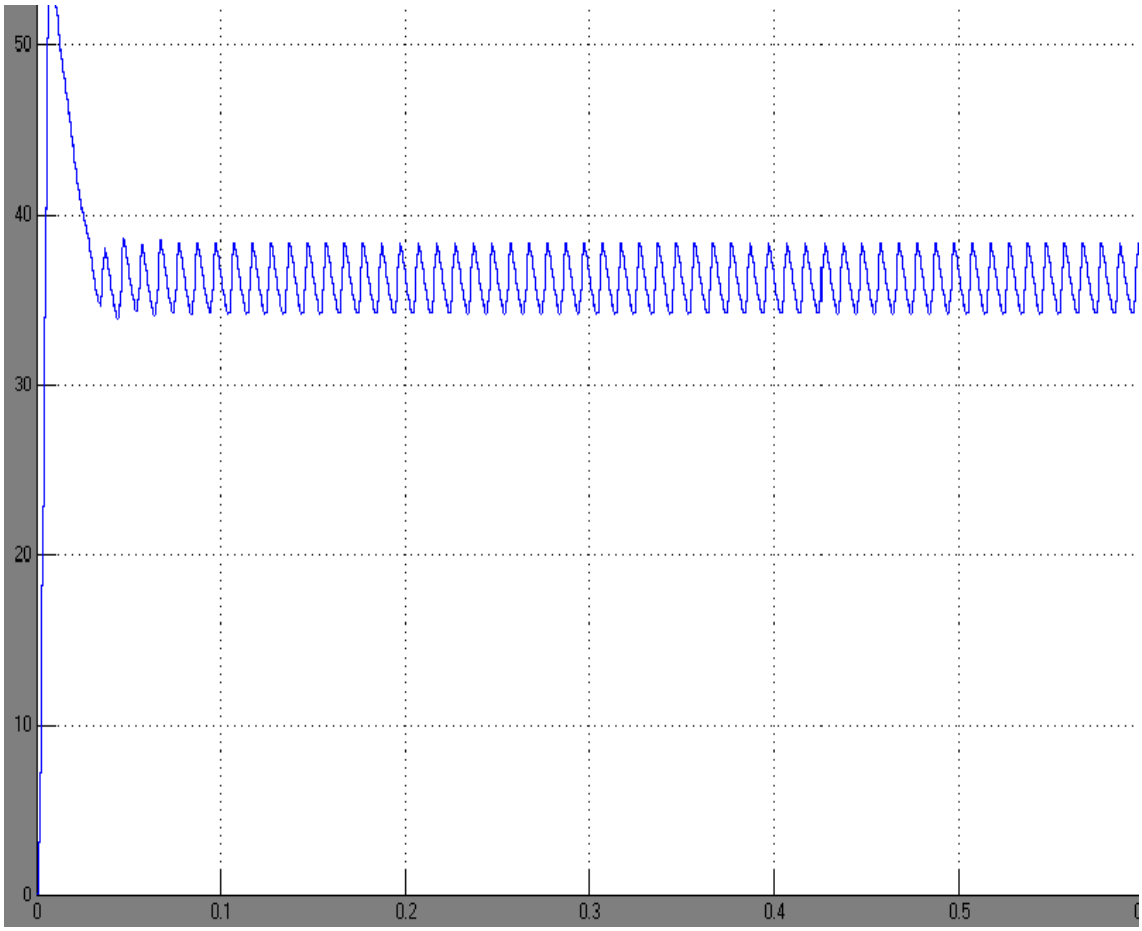


**Figure 4**. Output Voltage for Bridgeless Interleaved Boost Converter Power Factor Correction Circuit

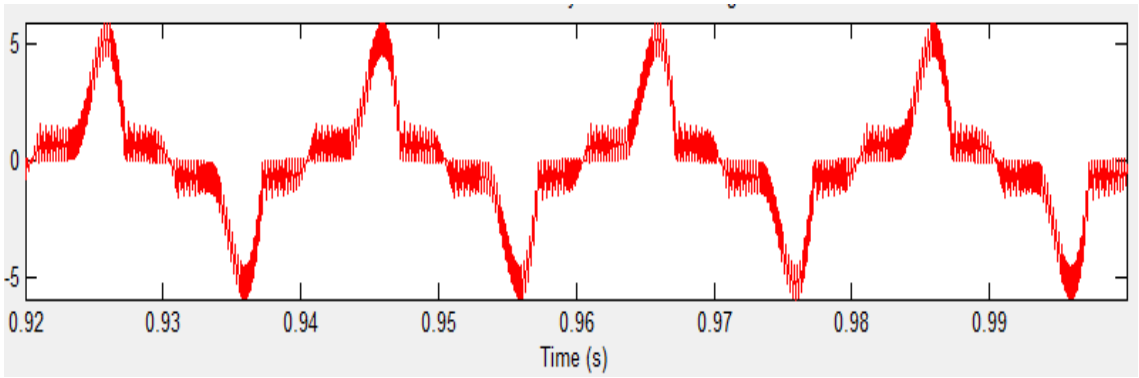


**Figure 5.** Waveform of input current.

Figure 5 shows the input current waveform of the proposed Bridgeless converter

## EXPERIMENTAL SETUP & RESULTS

### Description

A 15V - 0V - 15V step down transformer is used to step down the 230V AC supply from the mains to 15V for feeding the converter. The power circuit of the converter consists of four 667µH inductors, each of rating 5A which are used as boost inductors. It also consists of four MOSFETs – IRF840, manufactured by Vishay Intertechnology, Inc., Malvern, PA, United States, which are triggered using a 555 timer isolated from the power circuit using an Optocoupler MCT2E, manufactured by Texas Instruments,Dallas,United States. A filter capacitor of 1000µF is used to filter out the AC content in the output voltage and a 50 Ohm, 1W resistor is used as the load resistance.

### Generation of Triggering Pulses

A 555 timer is used for the generation of the pulses required to switch the MOSFETs ON and OFF. The power supply for the IC555 timer is provided with the help of a bridge rectifier and a regulator. A 7404 NOT gate is used in order to provide a phase shift of 180 degrees to the pulses which is used to trigger MOSFETs Q3 and Q4. The timer circuitry is designed to produce pulses with a frequency of 25kHz and 50% duty-cycle as shown in Figure 6 and Figure 7. The pictures illustrating the general purpose PCB of the timer circuit and the output of the timer are as follows

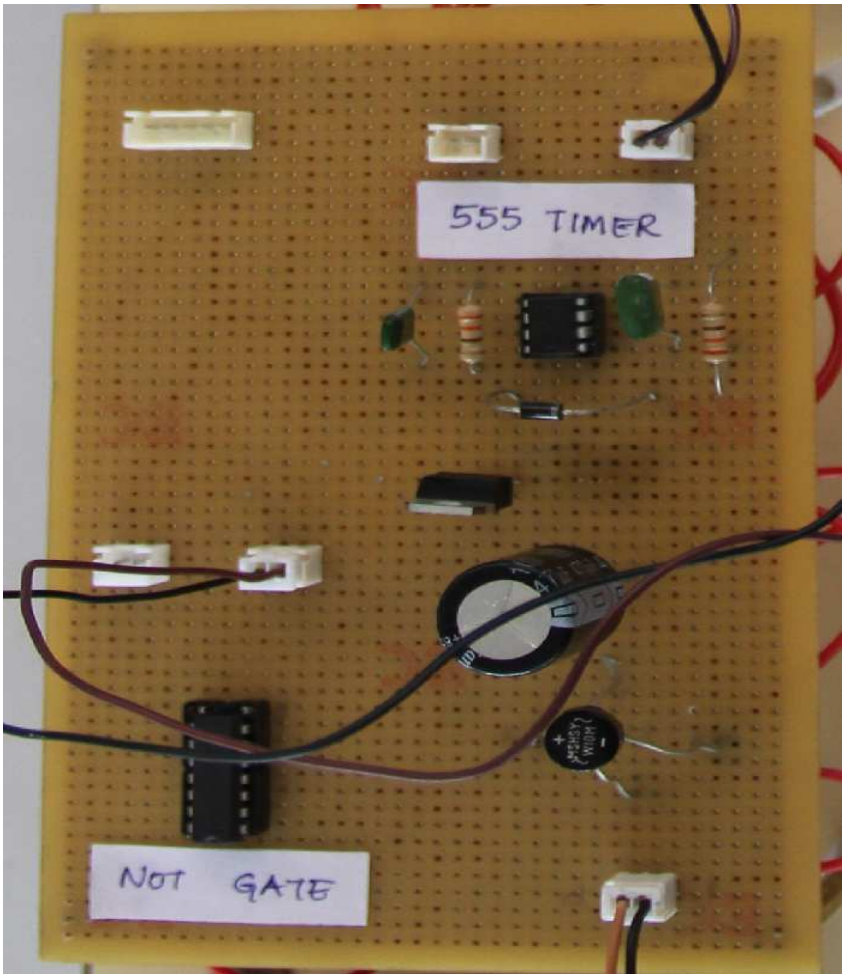


**Figure 6.** 555 timer Circuit

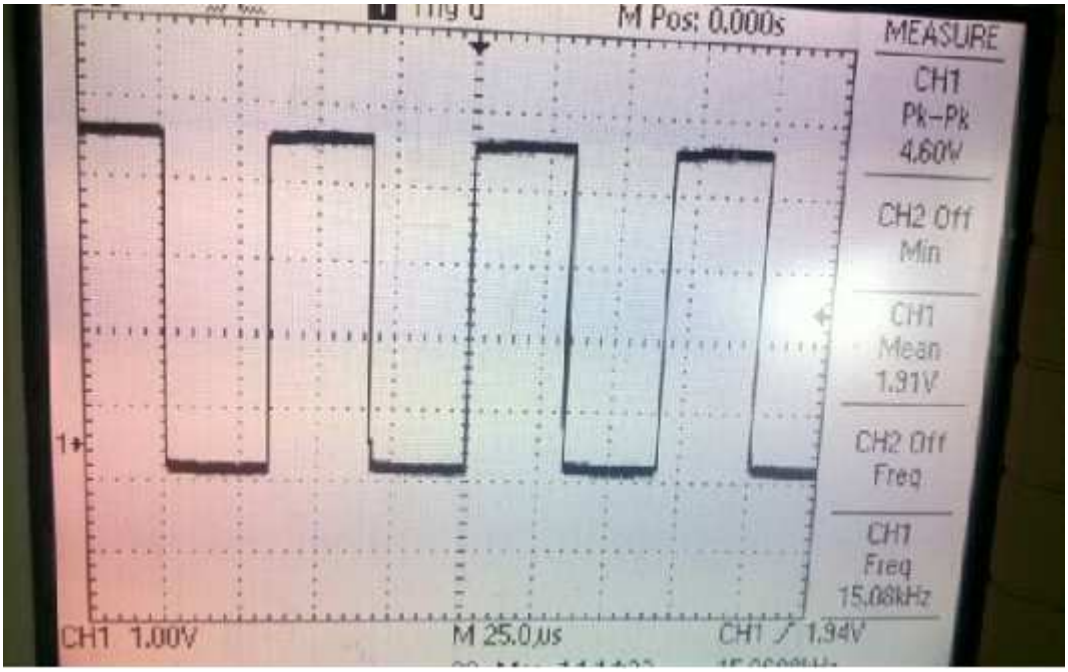


**Figure 7.** 555 timer output observed in a CRO

Figure 7 shows the gating pulses for the MOSFETS with 5 V amplitude, 25 kHz frequency and 50 % dutycyle.

**Timer Design Equations**

$$Time\ period = \frac{1}{frequency} \quad (4)$$

$$Duty\ Cycle = \frac{T_{high}}{T_{high} + T_{low}} \quad (5)$$

$$T_{high} = 0.693(R_1 + R_2)C \quad (6)$$

$$T_{low} = 0.693R_2C \quad (7)$$

**Table 3**: Timer Design

| | |
|---|---|
| Duty Cycle | 50 % |
| Frequency | 25000 Hz |
| Time Period | 0.00004 s |
| $T_{High}$ , $T_{Low}$ | 0.00002 s |
| $R_1$, $R_2$ | 2.5 k Ω |
| C | 0.01 µF |

## Optocoupler Circuit

The output pulses from the 555 timer are fed into the optocoupler circuit board. MCT2E optocoupler manufactured by Texas Instruments is used to couple the pulses from the 555 timer to the MOSFETs [2]. The power supply for MCT2E IC is made possible with the help of bridge rectifier and a regulator. The output of the optocoupler is fed to the gate terminals of the MOSFETs.

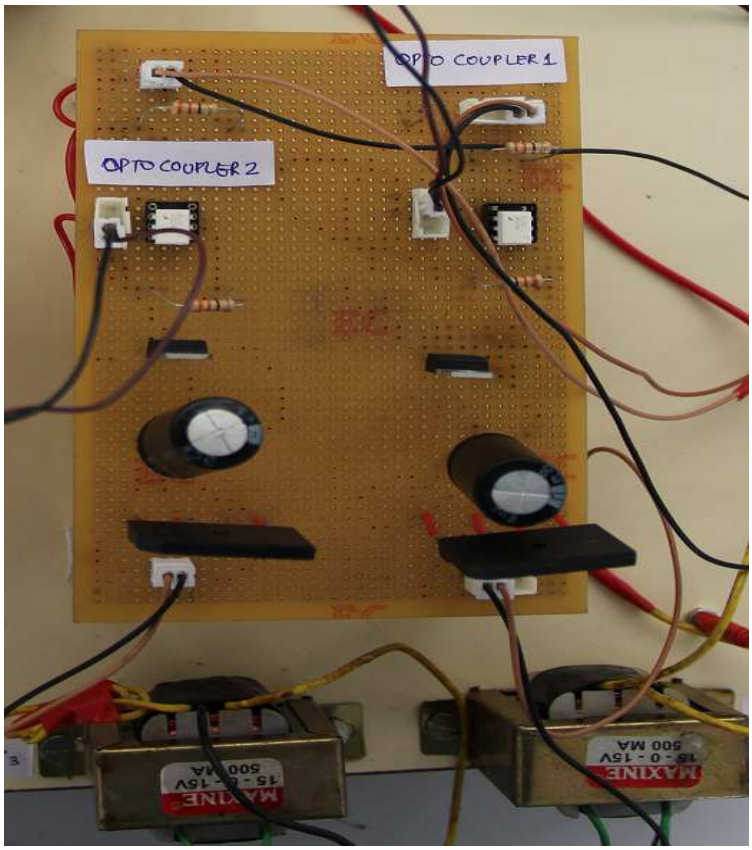


**Figure 8**. Optocoupler Circuit

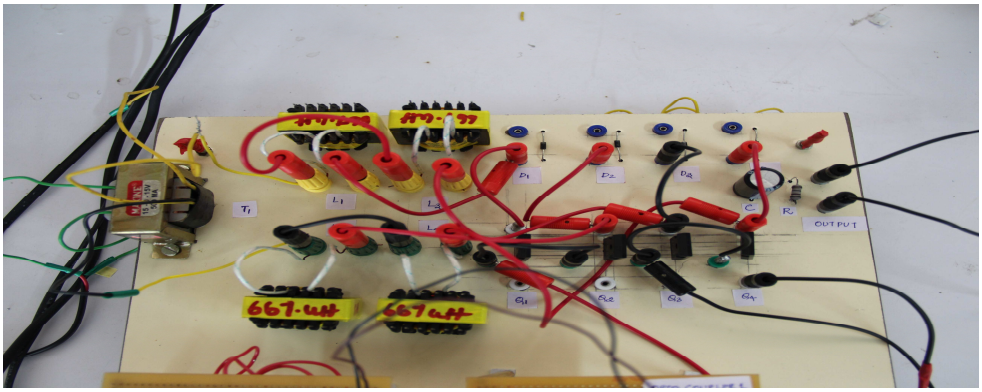


**Figure 9.** Power Circuit

The BLIL Prototype is as follows

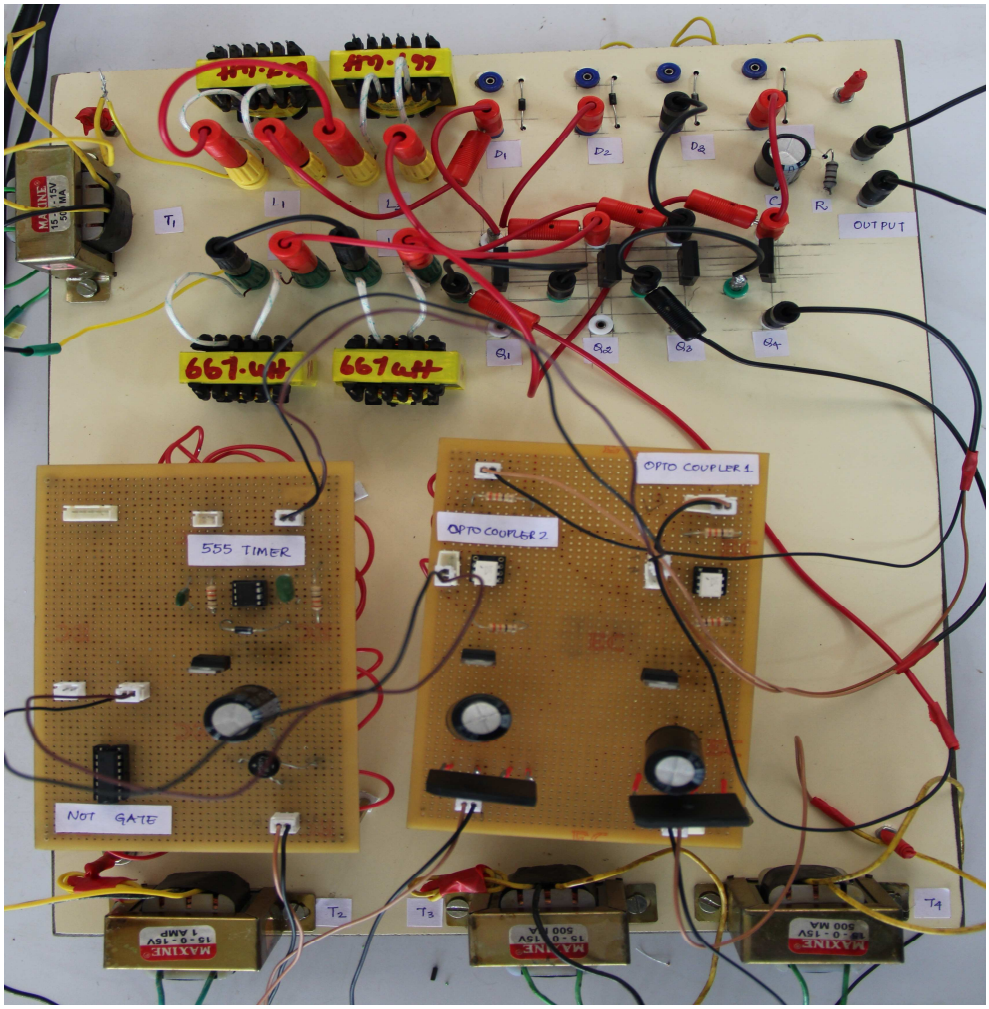


**Figure 10.** Bridgeless Interleaved Boost Converter PFC Circuit

## ANALYSIS


Figure 11. Input Voltage

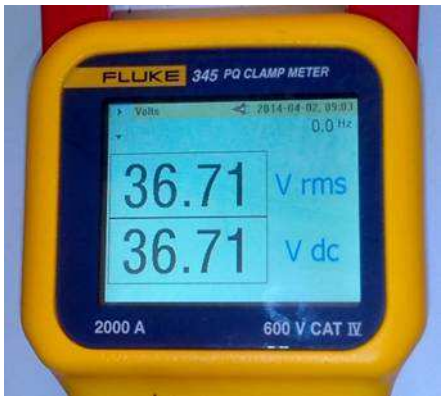


Figure 12. Output Voltage

The Input/Supply power factor was determined to be 0.974 using Power Quality Analyser.

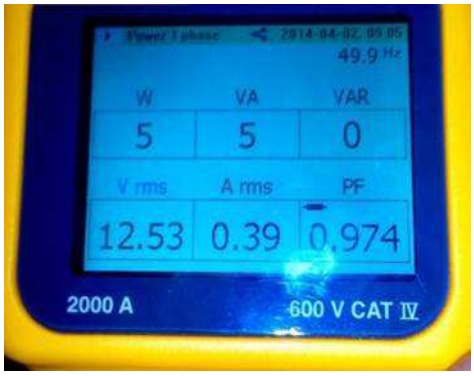


**Fig.13** Supply end Power Factor using PQ Analyzer

## CONCLUSION

A high performance Bridgeless Interleaved Boost converter with improved power factor for the front end hybrid electric charger has been presented in this paper. Hardware implementation of the proposed bridgeless configuration is built and also a detailed analysis on the performance of the developed topology was carried out to compare the theoretical results with the experimental results. The quality of the power delivered due to the implementation of the bridgeless power factor correction circuit is also verified using power quality analyzer. Therefore, the bridgeless configuration is a suitable front end topology for hybrid electric vehicles.

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